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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	Anthony M. Chiu
Serial No.	:	09/656,984
Filed	:	September 7, 2000
For	:	SURFACE MOUNT PACKAGE WITH INTEGRAL ELECTRO-STATIC CHARGE DISSIPATING USING LEAD FRAME AS ESD DEVICE
Group No.	:	2823
Examiner	:	K. D. Nguyen

BOX AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

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DOCKET NO. 00-C-016 (STMI01-00016) **PATENT**
Customer No. 30425

#10 / Appeal Brief
3/11/03
AS

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BOX AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

APPELLANTS' BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellants for the application identified above. A check is enclosed for the $320.00 fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

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REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC. (f/k/a SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 1–8 and 21–32 are pending in the present application. Claims 1–8, 21–25 and 29–31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,307,258 to *Crane, Jr. et al* in view of U.S. Patent No. 6,165,818 to *Ichikawa et al.* Claims 9–20 have been canceled pursuant to a restriction requirement. Claims 26–28 and 32 are objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all limitations of the base claim and any intervening claim(s). The rejection of pending claims 1–8, 21–25 and 29–31 is appealed.

STATUS OF AMENDMENTS

Following the final Office Action mailed August 14, 2002, claim 1 was amended solely to correct a typographical error. The Advisory Action mailed November 18, 2002 (Paper No. 7) indicates that the amendment will be entered upon appeal. No further amendments to the claims were submitted following the final Office Action.

SUMMARY OF THE INVENTION

The present invention relates to providing electrostatic discharge (ESD) protection for integrated circuits, particularly integrated circuits having a sensor area directly contacted by the user such as fingerprint detectors. Specification, page 2, lines 15–29. The present invention provides ESD protection by designing the lead frame to have portions which may be folded around edges of an encapsulated integrated circuit die. In an exemplary embodiment, several instances of the lead frame pattern are stamped or otherwise formed in a copper or other metal alloy lead frame strip 300:

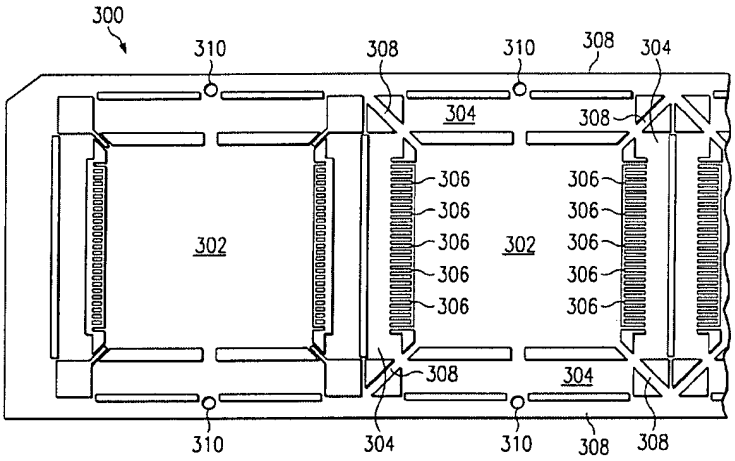

FIG. 3A

Specification, Figure 3A, page 7, line 31 through page 8, line2 and page 11, lines 4–12. The regions enclosed by solid lines within the lead frame strip 300 in Figure 3A are openings therethrough, portions that have been removed to pattern the strip 300. Each lead frame within the strip 300 within the strip includes a die paddle 302, to which the integrated circuit die will be affixed, regions

304 that will be folded around the encapsulated integrated circuit die as described in further detail below, lead portions 306 to which wire bonds from the integrated circuit die will be connected, and which will form the leads ("pins" or electrical connectors) to the packaged integrated circuit, and shorting bars 308, together with tooling (alignment) holes 310. Specification, page 11, lines 4–32.

During packaging of an integrated circuit, the ESD protection sections 304 will be folded around the sides of an encapsulated integrated circuit die affixed to die paddle 302 at fold lines 312 indicated in Figure 3B:

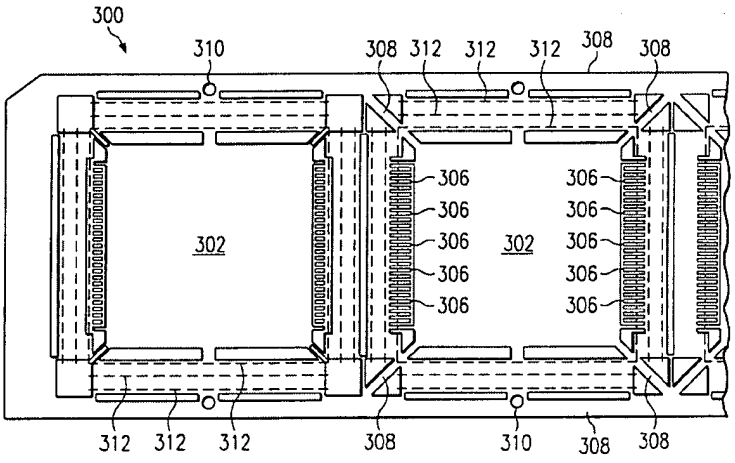

FIG. 3B

Specification, page 12, lines 1–9. These sections 304 remain physically and electrically connected to the die paddle 302 after folding to provide a ground connection.

During packaging, an integrated circuit die is mounted on the patterned lead frame, bond wires are affixed to connect bond sites on the integrated circuit die to the leads, and structure is (for example, mounted within a mold with the integrated circuit die and bond wires in the mold cavity

for injection encapsulation of the integrated circuit die and bond wires. Specification, page 7, lines 5–24. The individual lead frames within a strip may be separate before or after such encapsulation. A cross-sectional view of a packaged integrated circuit die according to the present invention is shown below:

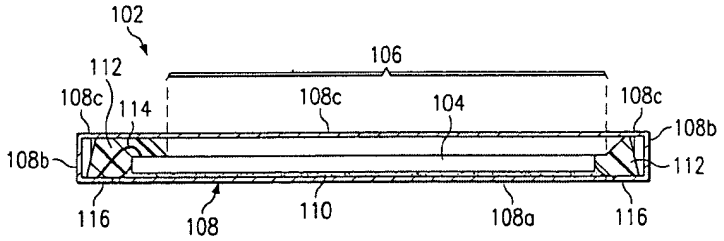

FIG. 1C

Specification, Figure 1C. Integrated circuit die 104 is affixed to the die paddle portion 108a of lead frame 108 by adhesive material 110; bond wires 114 connect the integrated circuit to leads or pins 116 (not visible in Figure 1C) formed from portions of lead frame 108; and a plastic or epoxy material encapsulates a portion of the integrated circuit die 104, bond wires 114, and a portion of lead frame 108. Specification, page 7, lines 5–24. Portions 108b and 108c of the lead frame 108 are then folded up around sides of the encapsulating material and over a peripheral upper surface of the encapsulating material to form an ESD ring. Specification, page 7, line 26 through page 8, line 2. Pins 116 are separated by trim and form operations (except possibly a ground connection pin 116a), but remain held in place by the encapsulating material 112, as best seen from the bottom view:

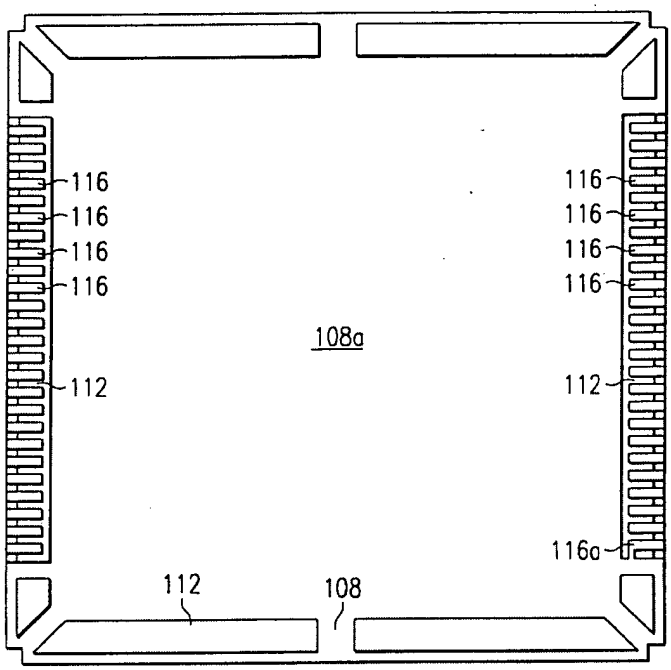

FIG. 1D

Specification, Figure 1D, page 8, lines 13–24. Pins 116 are thus physically and electrically separate from each other and from die paddle 108a, and may be used for signal connection to the packaged integrated circuit. Bond wires and pins may be employed on only one or on more than one side of the integrated circuit die. Specification, page 10, line 27 through page 11, line 2. The packaged integrated circuit is shown in perspective below:

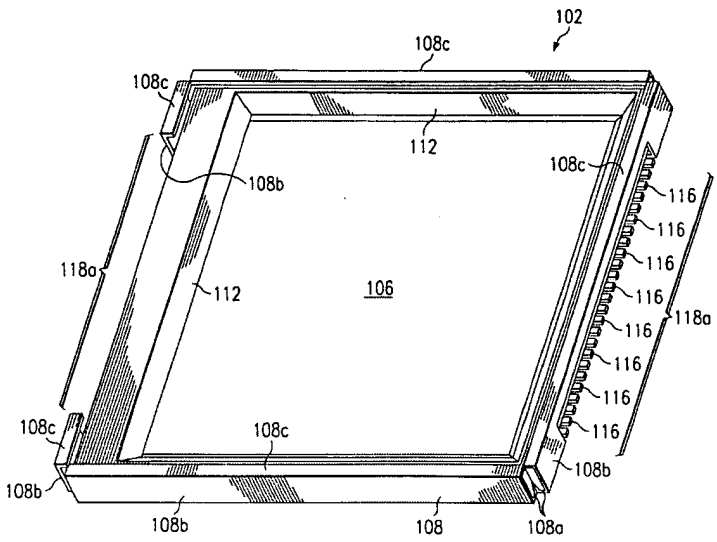

FIG. 1E

Specification, Figure 1E. Note that the portions 108c of lead frame 108 folded around the sides and over the peripheral upper surface of the encapsulating material may include portions over the area of connector pins 116 (as shown on the right of Figure 1E) or may alternatively include a complete gap at such regions (as shown on the left of Figure 1E), so that the resulting ESD ring may extend around an entire circumference of the peripheral upper surface of the packaged integrated circuit or around only a portion thereof. Specification, page 8, line 26 through page 9, line 9.

In the embodiment of Figures 1C–1E, pins 116 extended only to the outer edge of the packaged integrated circuit. In an alternative embodiment, however, the lead portions of the lead frame may be longer, so that after packaging the leads extend beyond an outer edge of the package

and may be shaped (bent) to form conventional "gull wing" leads for mounting the packaged integrated circuit on a printed circuit board:

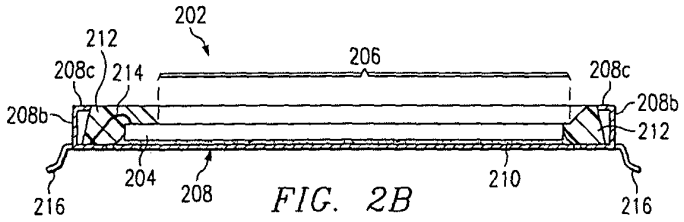

FIG. 2B

Specification, Figure 2B, page 10, lines 7–20. Even in this embodiment, however, an ESD ring is formed around at least some of the circumference of the package by folding lead frame portions up and around the sides.

In addition, the portion of the lead frame folded up and around the sides of the encapsulating material may be folded over a peripheral upper surface of the encapsulating material or, alternatively, merely folded so that portions 208c are proximate to and level with the peripheral upper surface of the encapsulating material 212 as shown in Figure 2B.

Various dimensions are possible with the claimed invention, such as an elongated package with folded regions along the long sides and pins (or leads or other connectors) along the short ends:

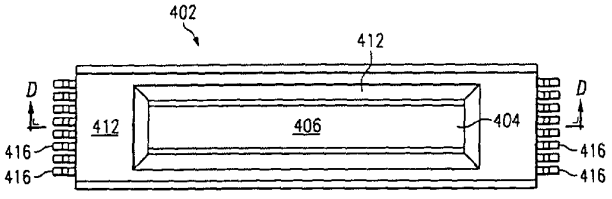

FIG. 4A

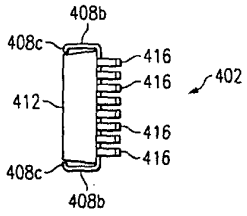

FIG. 4B

Specification, Figures 4A–4B, page 12, line 15 through page 13, line 17.

ISSUES ON APPEAL

Claims 1–8, 21–25 and 29–31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* The sole issue on appeal is whether claims 1–8, 21–25 and 29–31 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.*

GROUPING OF CLAIMS

Claims 1–8, 21–25 and 29–31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* For purposes of this appeal, the pending claims will be grouped together as follows:

Group A – claims 1–8, 21–25 and 29–31 (all pending rejected claims);

Group B – claim 2;

Group C – claim 3;

Group D – claim 4;

Group E – claim 5;

Group F – claim 6;

Group G – claims 7 and 30;

Group H – claim 8 and 31;

Group I – claim 22;

Group J – claim 24; and

Group K – claim 25.

Groups A–K stand or fall independently. Patentability of the claims within each group is argued separately below.

ARGUMENT

Group A

Claims 1–8, 21–25 and 29–31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* These claims are properly grouped together and considered separately from the claims of Groups B–K since they contain common limitations, and since a decision with respect to the claims of Group A may obviate the need for consideration of Groups B–K.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re*

Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

Independent claims 1, 21 and 29 recite, directly or indirectly, mounting an integrated circuit die on a lead frame. As the term is employed in the specification and within the ordinary meaning of the term with the relevant art, a lead frame is a structure formed (generally by stamping, although alternatively by milling or etching) from a metallic sheet, typically comprising a die paddle on which an integrated circuit die is mounted and lead portions extending outwardly therefrom to project from

the packaged integrated circuit after plastic or epoxy encapsulation of the integrated circuit die, die paddle, and part of each lead portion. The packaged integrated circuit leads are integrally formed from portions of the lead frame, shaped and separated during packaging by fold and trim operations.

Crane, Jr. et al teaches a housing 200 including separately formed insulative, polymeric sidewalls 210 and end plate 220 and (optionally conductive) cover plate 400:

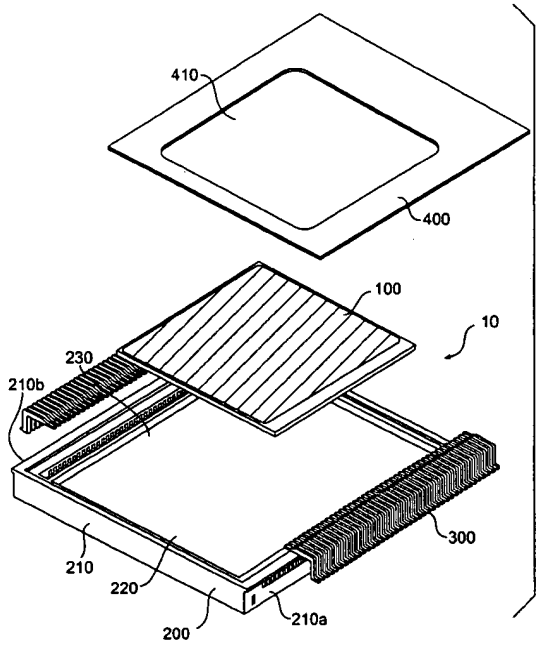

FIG. 1

Crane, Jr. et al, Figure 1. Leads 300 are separately formed from sidewalls 210 and end plate 220:

> FIGS. 1 and 2 illustrate one embodiment of a semiconductor die package 10 for holding a semiconductor die according to the present invention. FIG. 1 provides an exploded view of the semiconductor die package and semiconductor die shown in FIG. 2. As shown in FIGS. 1 and 2, semiconductor die package 10 includes a

> housing 200 for holding one or more semiconductor dies 100, leads 300 retained in the housing 200, and a cover plate 400 disposed at the top of the housing 200.
>
> The housing 200 includes a plurality of side walls 210 and an end plate 220. As shown in FIGS. 1 and 2, leads 300 extend from the side walls 210 of housing 200. While FIG. 2 shows a single row of leads 300 extending from opposite side walls 210a and 210b of housing 200, the leads 300 may extend from any one or more of the side walls 210 and may extend from the side wall(s) 210 in one or more rows.

Crane, Jr. et al, column 3, lines 56 through column 4, line 4. The sidewalls 210 and end plate 220 of housing 200 and leads 300 of *Crane, Jr. et al* therefore do not constitute a lead frame. *Crane, Jr. et al* is not analogous to the claimed invention (or to the teachings of *Ichikawa et al*, described below). *Ichikawa et al* alone of the cited references depicts and describes a lead frame 41 on which a "pellet" (an integrated circuit die) is mounted. *Ichikawa et al*, Figure 4, column 6, line 45 through column 7, line 25. In this respect, *Ichikawa et al* is at least analogous to the claimed invention.

With respect to the meaning of "lead frame," the Advisory Action asserts that limitations may not be read from the specification into the claims. However, the meaning of the term is both the ordinary meaning of that term to those skilled in the art and the meaning employed in the specification. Neither the final Office Action nor the Advisory Action offer any basis for concluding that the term should be given a different and/or broader meaning.

Independent claims 1, 21 and 29 also recite partially encapsulating at least part of the integrated circuit die and a portion of the leads formed from the lead frame. *Crane, Jr. et al* teaches encapsulating portions of an integrated circuit die 100 and conductive material connecting the die 100 to leads 300. *Crane, Jr. et al*, column 4, lines 25–27. However, *Crane, Jr. et al* does not depict

or describe a lead frame and is silent at to encapsulating a portion of a lead frame. *Ichikawa et al* alone of the cited references describes encapsulating the pellet mounted on a lead frame 41 and a portion of lead frame 41. *Ichikawa et al*, Figure 7, column 7, lines 27–39.

Independent claims 1, 21 and 29 each recite folding unencapsulated portions of the lead frame around the sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy encapsulating material. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* depicts and describes forming a cover plate 400 received by housing 200 over an encapsulated integrated circuit, where the cover plate 400 has an opening 410 therethrough for a fingerprint sensor and is optionally formed of conductive material to discharge static from a person's finger. *Crane, Jr. et al*, column 7, lines 25–45. However, *Crane, Jr. et al* is silent as to folding or wrapping a portion of a lead frame (or nonconductive housing 200) around an encapsulated integrated circuit die. *Ichikawa et al* also is silent as to folding or wrapping a portion of the lead frame around an encapsulated integrated circuit die.

At best, *Crane, Jr. et al* depicts an end structure loosely similarly to that produced by the claimed invention, but formed in a different manner. However, the claims under appeal are method claims, and similarity of the resulting structure is not relevant to obviousness of the claims, particularly since a materially different process is employed to produce that structure. *Ichikawa et al* teaches using some of the elements employed in the same invention, but not in the manner recited. Both references fail to depict or describe at least one step in the process recited: folding

unencapsulated portions of a base structure (whether the insulative, polymeric sidewalls 210 and end plate 220 of housing 200 in *Crane, Jr. et al* or the lead frame 41 in *Ichikawa et al*) BOTH around the sides of the encapsulated integrated circuit die AND over or adjacent to a peripheral upper surface of the plastic or epoxy encapsulating material. *Crane, Jr. et al* depict and describes preforming the sidewalls 210 of housing 200 *prior to* mounting and encapsulating the integrated circuit die rather than folding portions of the housing 200 around a mounted and encapsulated integrated circuit die *after* mounting and encapsulation. *Ichikawa et al* does not depict or describe folding the lead frame 41 around the sides of the mounted and encapsulated pellet.

The combined references fail to provide a motivation or incentive for modifying the respective teachings to achieve the claimed invention. The mere use of conventional lead frame technology in *Ichikawa et al* does not provide a motivation or incentive for employing such technology to produce a structure having conductive electrostatic discharge protection around a peripheral upper surface of a fingerprint sensor by folding portions of the lead frame to form the ESD protection. The use of a separate conductive cover plate to provide electrostatic discharge protection over a fingerprint sensor in *Crane, Jr. et al* does not provide a motivation or incentive to achieve similar results using lead frame technology and specifically by folding a portion of the lead frame, after mounting and encapsulating the integrated circuit die, up and around sides of the mounted and encapsulated integrated circuit die.

The combined references also fail to provide a reasonable expectation of success in achieving the claimed invention. Neither reference contains any teaching or suggestion that the respective packaging processes may be successfully combined. Neither reference contains any basis for expecting that the conventional lead frame technology employed in *Ichikawa et al* could be successfully modified to achieve the results produced by using a separate cover plate in *Crane, Jr. et al*. A general incentive (achieving a structure including an electrostatic discharge ring proximate to a sensing surface of a fingerprint sensor) does not render obvious a specific result (forming the electrostatic discharge ring from portions of a lead frame by folding those portions around sides of an encapsulated integrated circuit die mounted on the lead frame).

Crane, Jr. et al teaches a similar structure, but one formed by a very different method. *Ichikawa et al* relates to similar packaging processes, but without any suggestion that the processes could be successfully modified to achieve a structure similar to that produced in *Crane, Jr. et al*, or the specific claimed invention of forming the ESD protection integral with the lead frame and folding that ESD protection lead frame portion around the encapsulated integrated circuit. The references therefore fail to present a *prima facie* case of obviousness.

Group B

Claim 2 of Group B was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al*. This claim is considered separately from the claims of Groups A and C–K since it contains a limitation distinguishing the claim over the cited art not found in the

claims of Groups A and C–K: grounding the electrostatic discharge protection portion of the lead frame which is folded around the encapsulated integrated circuit die.

Claim 2 of Group B recites grounding the electrostatic discharge protection portion of the lead frame which is folded around the encapsulated integrated circuit die. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* does not depict or describe use of a lead frame, or folding of a lead frame around an encapsulated portion of an integrated circuit. *Crane, Jr. et al* does describe either grounding of some of leads 300 or, alternatively, connection of some leads 300 to optional ESD shielding:

> Not all of the leads 300 need to be electrically connected to the semiconductor die. Some of leads 300 may not be connected to any electrically conductive element within the housing 200. Alternatively or in addition, some of leads 300 may be electrically connected to electromagnetic interference (EMI) or electrostatic discharge (ESD) shielding either internal or external to the housing 200, a ground or power plane included within the housing 200, or another electrical component within the housing.

Crane, Jr. et al, column 4, lines 15–24. However, *Crane, Jr. et al* does not depict or describe grounded the cover plate 400, or connecting the cover plate 400 to a grounded lead 300 (whether directly or by connecting a lead electrically connected to ESD shielding to a lead connected to ground). *Ishikawa et al* similarly teaches grounding leads, but does not teach or suggest folding a portion of the lead frame around the encapsulated integrated circuit pellet to a location over or adjacent to a peripheral upper surface of the pellet, or grounding that portion folded around the encapsulated pellet.

Group C

Claim 3 of Group C was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* This claim is properly considered separately from the claims of Groups A–B and D–K since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–B and D–K: encapsulating exposed surfaces of an integrated circuit die mounted on a lead frame except for a sensing surface

Claim 3 of Group C recites encapsulating exposed surfaces of an integrated circuit die mounted on a lead frame except for a sensing surface. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* does not depict or describe using a lead frame in packaging a sensor circuit, and teach using a preformed insulative housing receiving the integrated circuit die and a conductive plate 400 and is silent as to using an encapsulant only over exposed surfaces of an integrated circuit die other than a sensing surface. *Ichikawa et al* does not teach or suggest encapsulating less than all of the pellet mounted on the lead frame. The references, taken alone or in combination, provide no motivation or incentive for combining the respective teachings to achieve the claimed invention, and no reasonable expectation of success that the respective teachings could be successfully combined to achieve the claimed invention.

Group D

Claim 4 of Group D was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* This claim is properly considered separately from the claims of

Groups A–C and E–K since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–C and E–K: folding portions around each side of the encapsulated integrated circuit die.

Claim 4 of Group D recites folding portions around each side of the encapsulated integrated circuit die. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* is silent at to folding a portion of any structure around the integrated circuit, or specifically folding a portion of any structure around all sides of the integrated circuit. *Ichikawa et al* does not teach or suggest folding portions of the lead frame around each side of the integrated circuit.

Group E

Claim 5 of Group E was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* This claim is properly considered separately from the claims of Groups A–D and F–K since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–D and F–K: folding a portion of the lead frame around one side of the encapsulated integrated circuit die, with the folded portion having an opening therein providing access to a connector to pins electrically connected to the integrated circuit die.

Claim 5 of Group E recites folding a portion of the lead frame around one side of the encapsulated integrated circuit die, with the folded portion having an opening therein providing access to a connector to pins electrically connected to the integrated circuit die. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* describes forming sidewalls 220 with

openings for individual leads 300, but does not describe leaving an opening therethrough for coupling of a connector to such leads. Moreover the references, taken alone or in combination, fail to provide a motivation or incentive for modifying the respective teachings to (a) fold the lead frame of *Ichikawa et al* to form structures equivalent to sidewalls 220, or (b) to fold the lead frame to form such structures with openings providing access for a connector (as opposed to merely passage of a portion of leads 300).

Group F

Claim 6 of Group F was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al*. This claim is properly considered separately from the claims of Groups A–E and G–K since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–E and G–K: folding lead frame portions around edges of the encapsulated integrated circuit other than edges of the lead frame including electrical leads for the integrated circuit.

Claim 6 of Group F recites that the folding of lead frame portions around the encapsulated integrated circuit does not include edges of the lead frame including electrical leads for the integrated circuit. Such a feature is not depicted or described by the cited references. Neither reference describes selecting only edges of a lead frame not including leads for folding around the encapsulated die to form an ESD protection ring.

Group G

Claims 7 and 30 of Group G were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* These claims are properly grouped together and considered separately from the claims of Groups A–F and H–K since they contain common limitations distinguishing the claims over the cited art not found in the claims of Groups A–F and H–K: that folding of the lead frame includes folding of a first portion around a side of the encapsulated integrated circuit die, and a second portion extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die.

Claims 7 and 30 of Group G recite that folding of the lead frame includes folding of a first portion around a side of the encapsulated integrated circuit die, and a second portion extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die. Such a feature is not depict or described by the cited references. *Crane, Jr. et al* describes separate sidewall and cover plate portions; *Ichikawa et al* does not teach folding anything except leads, and not around the side and over a peripheral upper surface of the encapsulated integrated circuit die.

Group H

Claims 8 and 31 of Group H were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* These claims are properly grouped together and considered separately from the claims of Groups A–G and I–K since they contain common limitations distinguishing the claims over the cited art not found in the claims of Groups A–G and

I–K: that folding of the lead frame includes folding of a first portion around a side of the encapsulated integrated circuit die, and a second portion extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

Claims 8 and 31 of Group H recite that folding of the lead frame includes folding of a first portion around a side of the encapsulated integrated circuit die, and a second portion extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* describes separate sidewall and cover plate portions; *Ichikawa et al* does not teach folding anything except leads, and not around the side and adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

Group I

Claim 22 of Group I was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al*. This claim is properly considered separately from the claims of Groups A–H and J–K since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–H and J–K: encapsulating only the integrated circuit die and the portion of the lead frame on which the integrated circuit die is mounted, leaving the remaining portions unencapsulated, including the surface of the lead frame portion opposite that on which the integrated circuit die is mounted.

Claim 22 of Group I recites encapsulating only the integrated circuit die and the portion of the lead frame on which the integrated circuit die is mounted, leaving the remaining portions, including the surface of the lead frame portion opposite that on which the integrated circuit die is mounted, unencapsulated. Such a feature is not depict or described by the cited references. *Crane, Jr. et al* does not relate to lead frames. *Ichikawa et al* does not teach or suggest encapsulating only one side of a lead frame portion on which the pellet is mounted. The references, taken alone or in combination, provide neither (1) motivation or incentive for forming the structure of *Crane, Jr. et al* using lead frame-based packaging or modifying the lead frame packaging process of *Ichikawa et al* to leave one surface of the lead frame portion on which the pellet is mounted unencapsulated, nor (2) a reasonable expectation of success that the respective teachings could be combined to achieve the claimed invention.

Group J

Claim 24 of Group J was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al.* This claim is properly considered separately from the claims of Groups A–I and K since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–I and K: mounting the integrated circuit die on a flat lead frame including leads projecting from at least one edge and an electrostatic discharge protection portion projecting from at least one edge.

Claim 24 of Group J recites mounting the integrated circuit die on a flat lead frame including leads projecting from at least one edge and an electrostatic discharge protection portion projecting from at least one edge. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* does not relate to lead frames. *Ichikawa et al* does not teach or suggest an electrostatic discharge portion projecting from one edge of a lead frame. The references, taken alone or in combination, provide no motivation for modifying the lead frame in *Ichikawa et al* to include an electrostatic discharge portion projecting from an edge thereof (recall that sidewalls 220 in *Crane, Jr. et al* are insulative, while leads 300 and cover portion 400 are separate), nor any reasonable expectation that such modification could be successfully achieved.

Group K

Claim 25 of Group K was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Crane, Jr. et al* in view of *Ichikawa et al*. This claim is properly considered separately from the claims of Groups A–J since it contains a limitation distinguishing the claim over the cited art not found in the claims of Groups A–J: that the electrostatic discharge portion extends from an edge of the lead frame other than an edge from which the leads project.

Claim 25 of Group K recites that the electrostatic discharge portion extends from an edge of the lead frame other than an edge from which the leads project. Such a feature is not depicted or described by the cited references. *Crane, Jr. et al* does not relate to lead frames. *Ichikawa et al* does not teach or suggest an electrostatic discharge portion projecting from any edge of a lead frame,

much less an edge other than that from which the leads project. The references, taken alone or in combination, provide no motivation for modifying the lead frame in *Ichikawa et al* to include an electrostatic discharge portion projecting from an edge thereof other than the edge from which the leads project (recall that sidewalls 220 in *Crane, Jr. et al* are insulative, while leads 300 and cover portion 400 are separate), nor any reasonable expectation that such modification could be successfully achieved.

CONCLUSION

None of the cited references, taken alone or in combination, depict or describe all features of the invention claimed in Groups A–K. Therefore, the rejection under 35 U.S.C. § 103 is improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1–8, 1–25 and 29–31 in this application.

Respectfully submitted,

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APPENDIX TO APPELLANT'S BRIEF ON APPEAL
PENDING CLAIMS ON APPEAL

1. A method of providing electrostatic discharge protection for an integrated circuit, comprising:

mounting an integrated circuit die on a lead frame;

encapsulating at least part of the integrated circuit die and a portion of the lead frame with a plastic or epoxy material; and

folding an unencapsulated portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material.

2. The method of claim 1, further comprising:

connecting the portion of the lead frame folded around the sides of the encapsulated integrated circuit die and over or adjacent to the peripheral upper surface of the plastic or epoxy material to a ground voltage.

3. The method of claim 1, wherein the step of encapsulating at least part of the integrated circuit die with a plastic or epoxy material further comprising:

after mounting the integrated circuit die on the lead frame, encapsulating exposed surfaces of the integrated circuit die except for a sensing surface; and

encapsulating wire bonds connecting the integrated circuit die to portions of the lead frame.

4. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding portions of the lead frame around each side of the encapsulated integrated circuit die.

5. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a first side of the encapsulated integrated circuit die, wherein the first portion includes an opening providing access for a connector to pins electrically connected to the integrated circuit die.

6. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding portions of the lead frame around edges of the encapsulated integrated circuit die not including leads electrically connected to the integrated circuit die.

7. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a side of the encapsulated integrated circuit die; and

folding a second portion of the lead frame extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die.

8. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a side of the encapsulated integrated circuit die; and

folding a second portion of the lead frame extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

Claims 9–20 canceled.

21. A method of providing electrostatic discharge protection for an integrated circuit, comprising:

encapsulating at least part of an integrated circuit die mounted on a lead frame and a portion of the lead frame with a plastic or epoxy material, leaving lead portions and an electrostatic discharge protection portion of the lead frame unencapsulated; and

folding the electrostatic discharge protection portion of the lead frame around the encapsulated integrated circuit die and over or adjacent to a surface of the plastic or epoxy material.

22. The method of claim 21, wherein the step of encapsulating at least part of an integrated circuit die mounted on a lead frame and a portion of the lead frame with a plastic or epoxy material, leaving lead portions and an electrostatic discharge protection portion of the lead frame unencapsulated further comprises:

forming the plastic or epoxy material over one surface and sidewalls of the integrated circuit die and over portions of a surface of the lead frame on which the integrated circuit die is mounted, leaving an opposite surface of the lead frame and the lead portions and the electrostatic discharge protection portion of the lead frame unencapsulated.

23. The method of claim 21, wherein the step of encapsulating at least part of an integrated circuit die mounted on a lead frame and a portion of the lead frame with a plastic or epoxy material, leaving lead portions and an electrostatic discharge protection portion of the lead frame unencapsulated further comprises:

leaving a contact surface of the integrated circuit die exposed.

24. The method of claim 21, further comprising:

mounting the integrated circuit die on a flat lead frame having the lead portions projecting from at least one edge and the electrostatic discharge protection portion projecting from at least one edge.

25. The method of claim 24, wherein the electrostatic discharge protection portion of the lead frame projects from an edge other than an edge from which the lead portions project.

26. The method of claim 24, wherein the electrostatic discharge protection portion of the lead frame projects from an edge from which the lead portions project, the electrostatic discharge protection portion extending around the lead portions and beyond ends of the lead portions.

27. The method of claim 24, wherein the electrostatic discharge protection portion of the lead frame projects from at least two opposing edges of the lead frame.

28. The method of claim 28, wherein the electrostatic discharge protection portion of the lead frame projects from at least three edges of the lead frame, including one edge from which the lead portions project.

29. A method of providing electrostatic discharge protection for an integrated circuit, comprising:

forming a flat lead frame having lead portions and an electrostatic discharge protection portion extending from edges thereof;

mounting an integrated circuit die on a surface of the lead frame and encapuslating the at least sides of the integrated circuit die and a portion of the lead frame surface on which the integrated circuit die is mounted with an encapsulating material, leaving the lead portions and the electrostatic discharge protection portion of the lead frame projecting beyond the encapsulating material;

folding the electrostatic discharge protection portion of the lead frame around one or more sides of the encapsulating material.

30. The method of claim 29, wherein the step of folding the electrostatic discharge protection portion of the lead frame around one or more sides of the encapsulating material further comprises:

folding the electrostatic discharge protection portion of the lead frame to extend along the sides of the encapsulating material; and

folding the electrostatic discharge protection portion of the lead frame to extend over a periphery of a surface of the encapsulating material opposite the lead frame.

31. The method of claim 29, wherein the step of folding the electrostatic discharge protection portion of the lead frame around one or more sides of the encapsulating material further comprises:

folding the electrostatic discharge protection portion of the lead frame to extend along the sides of the encapsulating material; and

folding the electrostatic discharge protection portion of the lead frame to extend adjacent to a surface of the encapsulating material opposite the lead frame.

32. The method of claim 29, wherein the step of folding the electrostatic discharge protection portion of the lead frame around one or more sides of the encapsulating material further comprises:

folding the electrostatic discharge protection portion of the lead frame around at least two opposing sides of the encapsulating material.